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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,000	09/27/2001	Van Hoa Lee	AUS920010672US1	2724

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EXAMINER	
LOHN, JOSHUA A	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,000	LEE ET AL.	
	Examiner	Art Unit	
	Joshua A Lohn	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-11, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forsman et al., United States Patent no. 6,742,139, filed October 19, 2000, in view of Chen, United States Patent no. 5,913,064, published June 15, 1999.

As per claim 1, Forsman discloses a method in a data processing system for testing hardware in a data processing system having multiple partitions (Forsman, col. 1, lines 32-48, where the service processor and the host represent the multiple partitions). Forsman discloses initializing a monitor process in a first partition assigned to a first processor (Forsman, col. 4, lines 9-24, where host is first processor) and to test the second processor (Forsman, col. 6, lines 13-14, where the service processor testing includes self testing), wherein the monitor process monitors the testing process and resets the second processors if the testing process fails (Forsman, col. 3, 19-41, where service processor is second processor). Forsman fails to disclose the testing process being a random code generation process

Chen discloses initializing a random code generation process, wherein the random code generation process generates instructions and executes the instructions to a processor (Chen, col. 1, lines 13-18).

It would have been obvious to one skilled in the art at the time of the invention to use the random code generation process of Chen in the testing system of Forsman.

This would have been obvious because Forsman discloses a need to monitor errors in processors (Forsman, col. 3, lines 20-25). Chen discloses that a well-known method to fully test the capabilities of a processor is random code generation (Chen, col. 1, lines 13-18). The implementation of the random code generation of Chen in the testing of Forsman would have resulted in the obvious benefit of fully testing the processor and improving the accuracy of the error monitoring.

As per claim 2, Forsman and Chen disclose that the random code generation process generates a heartbeat used by the monitor process to determine whether the random code generation process has failed (Forsman, col. 4, lines 9-24, where the service processor obviously executes the random code generation process).

As per claim 3, Forsman and Chen disclose the random code generation process calls a function to store data for the heartbeat in a data structure (Forsman, col. 4, lines 9-24, where the heartbeat signal is data stored in the structure of the heartbeat transmission signal).

As per claim 4, Forsman and Chen disclose the monitor process monitors the random code generation process by checking the data structure (Forsman, col. 4, lines 9-35, where the monitoring of the heartbeat checks the data structure that contains it).

As per claim 6, Forsman and Chen disclose that responsive to detecting an error executing the instructions in the second partition, preventing termination of the second partition (Forsman, col. 3, lines 26-36, where the service processor will save and report the detected error

information detected during analysis and will not terminate during this detection).

As per claim 7, Forsman discloses a data processing system comprising: a bus system; a communications unit connected to the bus system; a memory connected to the bus system (Forsman, Figure 1), wherein the memory includes a set of instructions (Forsman, col. 3, lines 10-25); and a processing unit connected to the bus system, wherein the processing unit executes the set of instructions to initialize a monitor process in a first partition assigned to a first processor (Forsman, col. 4, lines 9-24, where the host is the first partition). Forsman also discloses instructions to test the second processor (Forsman, col. 6, lines 13-14, where the service processor testing includes self testing) and in which the monitor process monitors the testing process and resets the second processors if the testing process fails (Forsman, col. 3, lines 19-41, where service processor is second processor). Forsman fails to disclose the testing process being a random code generation process

Chen discloses initializing a random code generation process, wherein the random code generation process generates instructions and executes the instructions to a processor (Chen, col. 1, lines 13-18).

It would have been obvious to one skilled in the art at the time of the invention to use the random code generation process of Chen in the testing system of Forsman.

This would have been obvious because Forsman discloses a need to monitor errors in processors (Forsman, col. 3, lines 20-25). Chen discloses that a well-known method to fully test the capabilities of a processor is random code generation (Chen, col. 1, lines 13-18). The

implementation of the random code generation of Chen in the testing of Forsman would have resulted in the obvious benefit of fully testing the processor and improving the accuracy of the error monitoring.

As per claim 8, Forsman discloses a data processing system for testing hardware in a data processing system has multiple partitions (Forsman, col. 1, lines 32-48, where the service processor and the host represent the multiple partitions). Forsman discloses a first initializing means for initializing a monitor process in a first partition assigned to a first processor (Forsman, col. 4, lines 9-24, where the host is the first processor) and second initializing means for initializing a testing process in a second partition associated with a second processor and executing instructions to test the second processor (Forsman, col. 6, lines 13-14, where the service processor testing includes self testing), and wherein the monitor process monitors the testing process and resets the second processors if the testing process fails. (Forsman, col. 3, lines 19-41, where the service processor is the second processor). Forsman fails to disclose the testing process being a random code generation process

Chen discloses initializing a random code generation process, wherein the random code generation process generates instructions and executes the instructions to a processor (Chen, col. 1, lines 13-18).

It would have been obvious to one skilled in the art at the time of the invention to use the random code generation process of Chen in the testing system of Forsman.

This would have been obvious because Forsman discloses a need to monitor errors in processors (Forsman, col. 3, lines 20-25). Chen discloses that a well-known method to fully test the capabilities of a processor is random code generation (Chen, col. 1, lines 13-18). The implementation of the random code generation of Chen in the testing of Forsman would have resulted in the obvious benefit of fully testing the processor and improving the accuracy of the error monitoring.

As per claim 9, Forsman and Chen disclose the random code generation process generates a heartbeat used by the monitor process to determine whether the random code generation process has failed (Forsman, col. 4, lines 9-24, where the service processor obviously executes the random code generation process).

As per claim 10, Forsman and Chen disclose the random code generation process calls a function to store data for the heartbeat in a data structure (Forsman, col. 4, lines 9-24, where the heartbeat signal is data stored in the structure of the heartbeat transmission signal).

As per claim 11, Forsman and Chen disclose monitor process monitors the random code generation process by checking the data structure (Forsman, col. 4, lines 9-35, where the monitoring of the heartbeat checks the data structure that contains it).

As per claim 13, Forsman and Chen disclose preventing means, responsive to detecting an error executing the instructions in the second partition, for preventing termination of the second partition (Forsman, col. 3, lines 26-36, where the service processor will save and report the detected error information detected during analysis and will not terminate during this

detection).

As per claim 14, Forsman discloses a computer program product in a computer readable medium for testing hardware in a data processing system (Forsman, col. 6, lines 35-47) having multiple partitions (Forsman, col. 1, lines 32-48, where the service processor and the host represent the multiple partitions). Forsman discloses first instructions for initializing a monitor process in a first partition assigned to a first processor (Forsman, col. 4, lines 9-24, where the host is the first processor), and second instructions for initializing a test process in a second partition associated with a second processor, wherein the test process generates instructions and executes the instructions to test the second processor (Forsman, col. 6, lines 13-14, where the service processor testing includes self testing) and wherein the monitor process monitors the test process and resets the second processors if the test process fails (Forsman, col. 3, lines 19-41, where the service processor is the second processor). Forsman fails to disclose the testing process being a random code generation process

Chen discloses initializing a random code generation process, wherein the random code generation process generates instructions and executes the instructions to a processor (Chen, col. 1, lines 13-18).

It would have been obvious to one skilled in the art at the time of the invention to use the random code generation process of Chen in the testing system of Forsman.

This would have been obvious because Forsman discloses a need to monitor errors in processors (Forsman, col. 3, lines 20-25). Chen discloses that a well-known method to fully test the capabilities of a processor is random code generation (Chen, col. 1, lines 13-18). The

implementation of the random code generation of Chen in the testing of Forsman would have resulted in the obvious benefit of fully testing the processor and improving the accuracy of the error monitoring.

Claims 5 and 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Forsman in view of Chen in further view of Tremblay, United States Patent no. 6,212,604, published April 3, 2001.

As per claim 5, Forsman and Chen fail to disclose the first and second processor are located in a single chip.

Tremblay discloses having a first and a second processor on a single chip (Tremblay, col. 3, lines 5-23).

It would have been obvious to one skilled in the art at the time of the invention to implement the two processors of Forsman and Chen on a single chip, as taught by Tremblay.

This would have been obvious because the system of Forsman and Chen has a memory system shared between the processor and service processor (Forsman, Figure 1). Tremblay discloses that access to a shared memory can be made more efficiently by implementing the two processors on the same chip and having automatic sharing of information between processors without having to go through external interfaces (Tremblay, col. 3, lines 24-48). It would have been obvious to improve the efficiency of the invention of Forsman and Chen by including the teachings of Tremblay.

As per claim 12, Forsman and Chen fail to disclose the first and second processor are located in a single chip.

Tremblay discloses having a first and a second processor on a single chip (Tremblay, col. 3, lines 5-23).

It would have been obvious to one skilled in the art at the time of the invention to implement the two processors of Forsman and Chen on a single chip, as taught by Tremblay.

This would have been obvious because the system of Forsman and Chen has a memory system shared between the processor and service processor (Forsman, Figure 1). Tremblay discloses that access to a shared memory can be made more efficiently by implementing the two processors on the same chip and having automatic sharing of information between processors without having to go through external interfaces (Tremblay, col. 3, lines 24-48). It would have been obvious to improve the efficiency of the invention of Forsman and Chen by including the teachings of Tremblay.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure is provided on attached form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua A Lohn whose telephone number is (703) 305-3188. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoleil can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAL

SCOTT BADERMAN
PRIMARY EXAMINER